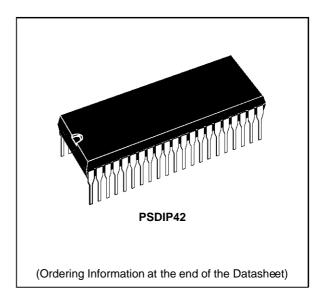


# DELECTRONICS ST9293 48K ROM HCMOS MCUs WITH ON SCREEN DISPLAY AND A/D CONVERTER

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- 16 to 48K bytes of ROM,
  256 to 768 bytes of RAM,
  224 general purpose registers available as RAM,
  accumulators or index registers (Register File)
- 42-lead Shrink DIP package
- Interrupt handler and Serial Peripheral Interface as standard features
- 31 fully programmable I/O pins
- 34 character x15 rows software programmable On Screen Display module with colour, italic, underline, flash, transparent and fringe attribute options
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- 16-bit programmable Slice Timer with 8-bit prescaler
- 4 channel Analog to Digital Converter, with integral sample and hold, fast 5.75µs conversion time, 6-bit guaranteed resolution
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed EPROM parts available for prototyping and pre-production development phases



FUNCTIONAL DESCRIPTION

## **DEVICE SUMMARY**

Device	ROM	RAM	PACKAGE
ST9293J7	48K	768	PSDIP42
ST9293J5	32K	640	PSDIP42
ST9293J3	24K	512	PSDIP42
ST9293J1	16K	256	PSDIP42

May 1993

This is Preliminary Data from SGS-THOMSON. Details are subject to change without notice.

#### 1.1GENERAL DESCRIPTION

The ST9293 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROM parts are fully compatible with their EPROM versions, which may be used for the prototyping and pre-production phases of development, and can be configured as standalone microcontrollers with 48K/32K/24K/16 bytes of onchip ROM.

The nucleus of the ST9293 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16-bit Timer/Watchdog with 8-bit Prescaler, a Serial Peripheral Interface supporting S-bus, I<sup>2</sup>C-bus and IM-bus Interface, plus two 8-bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set. The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9293 with up to 31/41 I/O lines dedicated to digital Input/Output.

These lines are grouped into up to six I/O Ports and can be configured on a bit basis under software

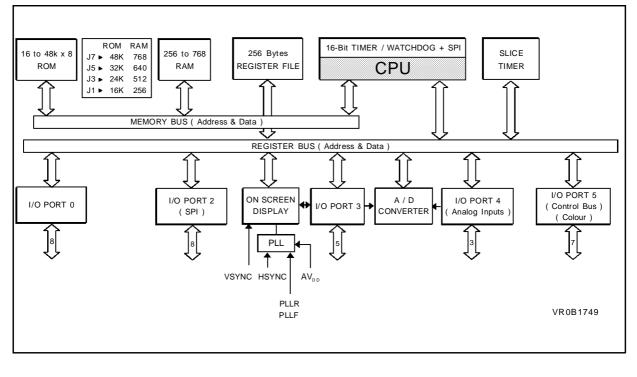
control to provide timing, status signals, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O.

Three basic memory spaces are available to support this wide range of configurations: Program Memory, Data Memory and the Register File, which includes the control and status registers of the on-chip peripherals.

The 16-bit Slice Timer with an 8-bit Prescaler and 6 operating modes allows simple use for waveformgeneration and measurement, PWM functions and many other system timing functions.

The human interface is provided by the On Screen Display module, this can produce up to 8 lines of of up to 34 characters from a ROM defined 128 character set. The 9x13 character can be modified by 4 different pixel sizes, with character rounding, and formed into words with colour and format attributes.

In addition there is a 4 channel Analog to Digital Converter with integral sample and hold, fast 5.5µs conversion time and 6-bit guaranteed resolution.



## Figure 1-1. ST9293 Block Diagram

## **1.2 PIN DESCRIPTION**

**VSYNC**. *Vertical Synch*. Vertical video synchronisation input to OSD. Positive or negative polarity.

**HSYNC**. *Horizontal Synch*. Horizontal video synchronisation input to OSD. Positive or negative polarity.

**PLLF**. *PLL Filter input.* Filter input for the OSD for PLL feed-back.

**PLLR**. *PLL Resistor connection pin.* For resistor connection to select the PLL gain adjust.

**RESET**. *Reset (input, active low)*. The ST9 is initialised by the Reset signal. With the deactivation of RESET, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

**OSCIN, OSCOUT**. Oscillator (input and output). These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.  $AV_{DD}$ . Analog  $V_{DD}$  of PLL. This pin must be tied to  $V_{DD}$  externally to the ST9293.

**V**<sub>DD</sub>. Main Power Supply Voltage (5V±10%)

**Vss, Vss2**. Digital Circuit Ground, these pins must be connected together externally to the ST9293.

**P0.0-P0.7**, **P2.0-P2.7**, **P3.3-P3.7**, **P4.5-P4.7**, **P5.0-P5.6** *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 31 lines grouped into I/O ports, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

P3.3 and P3.4 are true 12V open drain outputs when set in output mode.

## 1.2.1 I/O Port Alternate Functions.

Each pin of the I/O ports of the ST9293 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Table 1 shows the Functions allocated to each I/O Port pin.

I/O PORT	Name	Function	Alternate Function	Pin Assignment
Port.bit				9293J
P0.0		I/O		12
P0.1		I/O		11
P0.2		I/O		10
P0.3		I/O		9
P0.4		I/O		8
P0.5		I/O		7
P0.6		I/O		6
P0.7		I/O		5
P2.0	INT6	I	External Interrupt 6	39
P2.1	INT7	I	External Interrupt 7	40
P2.2	INT0	I	External Interrupt 0	41

Table 1-1. ST9293 I/O Port Alternate Function Summary



# PIN DESCRIPTION (Continued)

## Table 1-2. ST9293 I/O Port Alternate Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment
Port.bit				9293J
P2.3	INT3	I	External Interrupt 3	42
P2.4	WDOUT	0	T/WD Output	1
P2.4	EXTRG	I	External A/D Trigger	1
P2.5	SDO	0	MSPI Serial Data Output	2
P2.6	INT2	I	External Interrupt 2	3
P2.6	SCK	0	SPI Serial Clock	3
P2.7	SDO	0	SPI Serial Data Output	4
P2.7	SDI	I	SPI Serial Data Input	4
P3.3		0	(12V Open Drain Output)	34
P3.3	SLOUT	0	Slice Timer Output	34
P3.4		0	(12V Open Drain Output)	35
P3.4	SLIN	I	Slice Timer Input	35
P3.5	INT4	I	Schmitt Triggered Input Only	36
P3.6	WDIN	I	T/WD Input	37
P3.6	AIN4	I	A/D Analog Input 4	37
P3.7	NMI	I	Non-Maskable Interrupt	38
P4.5	AIN5	I	A/D Analog Input 5	27
P4.6	AIN6	I	A/D Analog Input 6	28
P4.7	AIN7	I	A/D Analog Input 7	29
P5.0		I/O		14
P5.1		I/O		15
P5.2		I/O		16
P5.3	FB	0	Fast Blanking OSD output	17
P5.4	В	0	Blue Video Colour OSD output	18
P5.5	G	0	Green Video Colour OSD output	19
P5.6	R	0	Red Video Colour OSD output	20

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